1. (Currently Amended) A method for accelerating the generation of control signals in a microcode controller system including a microcode controller, a microcode memory, [[an]] a level-sensitive address latch and a level sensitive code word latch, the method comprising:

opening the address latch during one of a high level and a low level [[the second half]] of a clock cycle to store therein an address decoded by the microcode controller, while simultaneously closing the code word latch during the second half of a clock cycle;

presenting the address stored in the address latch to the microcode memory to read out a code word therefrom;

opening the code word latch during [[the first half]] the respective other of the high level and the low level of a clock cycle to store the code word read out from the microcode memory to the code word latch, while simultaneously closing the address latch [[during the first half of a clock cycle]]; and

presenting the code word stored in the code word latch to the microcode controller for generation of output control signals and decoding at least one address.

2. (Currently Amended) A microcode controller system comprising:

control means for generating control signals and decoding address data;

means for latching address data decoded by the control means, said means for latching address data opening during [[the second half]] a second one of a high level and a low level of a clock cycle to store therein said decoded address data;

means for latching code word data, said means for latching code word data closing during the second half of a clock cycle, simultaneous with the opening of the means for latching address data; and

means for storing code word data, wherein code word data is read out of the means for storing code word data in response to presentation thereto of the address data stored in the address latch,

wherein said means for latching code word data opens during the first [[half]] one of the high level and the low level of a clock cycle to store the code word data read out from the means for storing code word data, and said means for latching address data simultaneously closes during the first [[half]] one of the high level and the low level of a clock cycle, said control means generating control signals and decoding at least one address, using the code word data stored in the means for latching code word data.

3. (Currently Amended) A microcode controller system comprising:

a microcode controller for generating control signals and decoding address data;

[[an]] a level-sensitive address latch for storing address data decoded by the microcode controller, said address latch opening during [[the second half]] a low level of a clock cycle to store said decoded address data therein;

a level sensitive code word latch for storing code word data, said code word latch closing during the [[second half]] low level of a clock cycle, simultaneous with the opening of the address latch; and

a microcode memory, wherein code word data is read out of the microcode memory in response to presentation thereto of the address data stored in the address latch,

wherein said code word latch opens during the [[first half]] high level of a clock cycle to store the code word data read out from the microcode memory, and said address latch simultaneously closes during the [[first half]] high level of a clock cycle, said microcode controller generating control signals and decoding at least one address, using the code word data stored in the code word latch.

4. (Currently Amended) A method for accelerating the generation of control signals in a microcode controller system including a microcode controller, a microcode memory, [[an]] a level-sensitive address latch and a level-sensitive code word latch, the method comprising:

opening the address latch during [[the second half]] a low level of a clock cycle to store therein an address decoded by the microcode controller, and closing the address latch during [[the first half]] a high level of a clock cycle;

presenting the address stored in the address latch to the microcode memory to read out a code word therefrom;

presenting the code word read out from the microcode memory to the microcode controller, said microcode controller generating output control signals and decoding at least one address from said presented code word.

5. (Currently Amended) A microcode controller system comprising:

control means for generating control signals and decoding address data;

means for latching address data decoded by the control means, said means for latching address data opening during [[the second half]] a low level of a clock cycle to store therein said decoded address data, and closing during [[the first half]] a high level of a clock cycle; and

means for storing code word data, wherein code word data is read out of the means for storing code word data in response to presentation thereto of the address data stored in the means for latching address data, wherein said code word data read out from the means for storing code word data is presented to said control means for generating control signals and decoding address data.

6. (Currently Amended) A microcode controller system comprising:

a microcode controller for generating control signals and decoding address data;

[[an]] a level-sensitive address latch for latching address data decoded by the microcode controller, said address latch opening during [[the second half]] one of a high level and a low level of a clock cycle to store therein said decoded address data, and closing during the [[first half]] respective other of the high level and the low level of a clock cycle;

a code word memory for storing code word data, wherein code word data is read out of the code word memory in response to presentation thereto of the address data stored in the address latch, wherein said code word data read out from the code word memory is presented to said microcode controller to generate control signals and decode address data.

7. (Currently Amended) A method for accelerating the generation of control signals in a microcode controller system including a microcode controller, a microcode memory, [[an]] a level-senistive address latch and a level sensitive code word latch, the method comprising:

presenting an address decoded by the microcode controller to the microcode memory to read out a code word therefrom;

opening the code word latch during the [[first half]] one of a high level and a low level of a clock cycle to store the code word read out from the microcode memory to the code word latch, and closing the code word latch during the [[second half]] respective other of the high level and the law level of the clock cycle; and

presenting the code word stored in the code word latch to the microcode controller for generation of output control signals and decoding at least one address.

8. (Currently Amended) A microcode controller system comprising:

control means for generating control signals and decoding address data;

means for latching code word data, said means for latching code word data closing during [[the second half]] a low level of a clock cycle; and

means for storing code word data, wherein code word data is read out of the means for storing code word data in response to presentation thereto of the address data decoded by the control means,

wherein said means for latching code word data opens during [[the first half]] a high level of a clock cycle to store the code word data read out from the means for storing code

word data, said control means generating control signals and decoding at least one address, using the code word data stored in the means for latching code word data.

9. (Currently Amended) A microcode controller system comprising:

a microcode controller for generating control signals and decoding address data;

a level-sensitive latch for storing code word data, said latch closing during [[the second half]] a low level of a clock cycle; and

a memory for storing code word data, wherein code word data is read out of the memory in response to presentation thereto of the address data decoded by the microcode controller,

wherein said latch opens during [[the first half]] a high level of a clock cycle to store the code word data read out from the memory, said microcode controller generating control signals and decoding at least one address, using the code word data stored in the latch.

10. (Original) A method for accelerating the generation of control signals in a microcode controller system including a microcode controller and a dual read port microcode memory having (1) a first read port comprised of: (a) a first read address port and (b) a first read data port, and (2) a second read port comprised of: (a) a second read address port and (b) a second read data port, the method comprising:

presenting an address decoded by the microcode controller to the first read address port, to read out a code word from the first read data port;

generating microcode control signals at the microcode controller using the code word from the first data output port;

generating a next address at the microcode controller using the code word from the first data output port;

presenting the next address to the second read address port to read out a next code word from the second read data port; and

alternating use of the first and second read ports for every other clock cycle.

11. (Original) A system for accelerating the generation of control signals in a microcode controller system including:

a microcode controller for decoding addresses and generating microcode control signals; and

a dual read port microcode memory having:

(1) a first read port comprised of: (a) a first read address port and (b) a first read data port, and

(2) a second read port comprised of: (a) a second read address port and (b) a second read data port,

wherein an address decoded by the microcode controller is presented to the first read address port, to read out a code word from the first read data port, said microcode controller using the code word from the first data output port to generate microcode control signals and generate a next address, wherein said next address is presented to the second read address port to

read out a next code word from the second read data port, said first and second read ports are alternately read from every other clock cycle.

12. (Original) A system for accelerating the generation of control signals in a microcode controller system including:

processing means for decoding addresses and generating microcode control signals; and

means for storing code words having a dual read port, said means for storing code words including:

(1) a first read port comprised of: (a) a first read address port and (b) a first read data port, and

(2) a second read port comprised of: (a) a second read address port and (b) a second read data port,

wherein an address decoded by the processing means is presented to the first read address port, to read out a code word from the first read data port, said processing means using the code word from the first data output port to generate microcode control signals and generate a next address, wherein said next address is presented to the second read address port to read out a next code word from the second read data port, said first and second read ports are alternately read from every other clock cycle.

13. (Currently Amended)A method for accelerating the generation of control signals in a pipelined microcode controller system including a microcode controller, a microcode

memory, a plurality of level-sensitive address latches and a plurality of level-sensitive code word latches, and having a plurality of clock cycle phases, the method comprising:

(a) opening a code word latch during the Nth phase of the clock cycle to store code word data therein read out from the microcode memory;

(b) closing said code word latch during the N+1 phase of the clock cycle, simultaneous with the opening of an address latch, wherein said address latch opens during the N+1th phase of a clock cycle to store address data read out from the microcode memory for the subsequent phase of the clock cycle after the N+1th phase of the clock cycle; and

repeating steps (a) and (b) with alternating phases of the clock cycle for respective opening and closing of the address latch and code word latch for a plurality of phases of the clock cycle, wherein the alternating phases are each respectively one of high-level or low level.

14. (Currently Amended) A system for accelerating the generation of control signals in a pipelined microcode controller system having a plurality of clock cycle phases including:

a microcode controller for decoding addresses and generating microcode control signals;

a microcode memory for storing code word data;

a plurality of level-sensitive address latches associated with the microcode controller and microcode memory; and

a plurality of level-sensitive code word latches associated with the microcode controller and microcode memory,

wherein (a) a code word latch is opened during the Nth phase of the clock cycle to store code word data therein read out from the microcode memory, (b) the code word latch is closed during the N+1 phase of the clock cycle, simultaneous with the opening of an address latch, wherein said address latch opens during the N+1th phase of a clock cycle to store address data from the microcode controller for the subsequent phase of the clock cycle after the N+1th phase of the clock cycle, wherein steps (a) and (b) are repeated with alternating phases of the clock cycle for respective opening and closing of the address latch and code word latch for a plurality of phases of the clock cycle, wherein the alternating phases are each respectively one of high-level or low level.

15. (Currently Amended) A system for accelerating the generation of control signals in a pipelined microcode controller system having a plurality of clock cycle phases including:

processing means for decoding addresses and generating microcode control signals;

means for storing code word data;

a plurality of means for level-sensitive latching address data; and

a plurality of means for level- sensitive latching code word data,

wherein (a) a means for latching code word data is opened during the Nth phase of the clock cycle to store code word data therein read out from the microcode memory, (b) the means for latching code word data is closed during the N+1 phase of the clock cycle, simultaneous with the opening of a means for latching address data, wherein said means for

latching address data opens during the N+1th phase of a clock cycle to store address data from the processing means for the subsequent phase of the clock cycle after the N+1th phase of the clock cycle, wherein steps (a) and (b) are repeated with alternating phases of the clock cycle for respective opening and closing of the means for latching address data and means for latching code word data, for a plurality of phases of the clock cycle, wherein the alternating phases are each respectively one of high-level and low-level.